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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/722,434 | 11/28/2003 | Takayuki Kondo | 117601 | 7369 |

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

| EXAMINER | |
|---|---|
| PALMER, PHAN T H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2874 | |

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/722,434 | KONDO, TAKAYUKI | |
| | Examiner | Art Unit | |
| | PHAN T.H. PALMER | 2874 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *18-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-29* is/are allowed.

6)☒ Claim(s) *18,20,21,25,26,32 and 33* is/are rejected.

7)☒ Claim(s) *19,22-24,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Phan T. H. Palmer
PHAN T. H. PALMER
PRIMARY EXAMINER
11/13/2005

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## ***DETAILED ACTION***

### *Claim Rejections - 35 USC § 102*

**1.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18, 20-21, 25-26, and 32-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Blondeau et al. (5,262,656).

The Blondeau et al. discloses on figure 2, an on-chip optical interconnection circuit, comprising:

- a first circuit block (L) provided on an integrated circuit chip, said first circuit block including a first element having a light emitting function (laser) provided on the first circuit block;

- a second circuit block (DEC) provided on the integrated circuit chip, said first circuit block including a second element having a light receiving function (detector) provided on the second circuit block; and

- an optical waveguide being provided on the integrated circuit chip, the first circuit block being connected to the second circuit block through the optical waveguide, and the optical waveguide being in contact with the first element and with the second element.

With regard to claim 18, the Blondeau et al discloses all the claimed invention.

With regard to claim 20, the on-chip optically interconnection circuit comprising the first element electrically connected to the first circuit block and optically connected to the optical waveguide, the second element electrically connected to the second circuit block and optically connected to the optical waveguide. Theses limitations are inherently disclosed in the Blondeau et al reference, since the elements within blocks L and DEC must have electrical interconnections in order to operate.

With regard to claim 21, the claimed invention is also disclosed in the Blondeau et al reference, since the waveguide at least partially covers the elements from below.

With regard to claims 25 and 26, are inherently disclosed in the Blondeau et al., since they merely recite uses of the device, which would certainly be obvious uses.

With regard to claims 32, and 33, are also disclosed in the Blondeau et al reference, since these claims do not add any further limitations.

***Allowable Subject Matter***

**2.** Claims 19, 22-24, and 30-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Blondeau et al reference does not disclose the first circuit block and the second circuit block being electrically connected to each other, as discloses in claim 19.

The Blondeau et al reference does not disclose at least a portion of the optical waveguide being provided on top surface of the first circuit block and the second circuit block, as discloses in claim 22.

The Blondeau et al reference does not disclose at least a portion of the optical waveguide crossing at least one of the first circuit and the second circuit, as discloses in claim 23.

The Blondeau et al reference does not disclose at least a portion of the optical waveguide being provided to bypass the first circuit and the second circuit, as discloses in claim 24.

The Blondeau et al reference does not disclose the optical waveguide including a light scattering frame scattering a light, emitted by the first elements, as discloses in claim 30.

The Blondeau et al reference does not discloses the optical waveguide including a light reflecting frame reflecting a light, emitted by the first elements, as discloses in claim 31.

**Claims 27-29 are allowed.**

The Blondeau et al reference does not disclose:

An on-chip optical interconnection circuit, comprising:

- a plurality of circuit blocks provided on an integrated circuit chip;

- a plurality of optical waveguides; and

- a plurality of elements having a light emitting function or a light receiving function;

the plurality of circuit blocks being optically connected to each other through at least one of the plurality of optical waveguides,

the plurality of elements electrically connected to the plurality of circuit blocks and optically connected to the plurality of optical waveguides;

two or more elements of the plurality of elements provided on one of the plurality of circuit blocks, and

at least one of the plurality of optical waveguides being provided for each of the two or more elements, as discloses in claims 27 and 28.

## CONTACT INFORMATION

**5.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHAN T.H. PALMER whose telephone number is (571) 272-2354. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RODNEY B. BOVERNICK can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**PTHP**
**11/13/2005**

Phan T. H. Palmer

**PHAN T. H. PALMER**
**PRIMARY EXAMINER**